An Efficient Approach for Large-Signal Modeling and Analysis of the GaAs MESFET

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Abstract—**A nonlinear circuit model of the GaAs MESFET is developed by extracting circuit parameters from dc and small-signal RF measurements in a systematic manner. The circuit model is then analyzed by an efficient algorithm called the modified multiple-reflection method. For the first time, this method is applied to MESFET circuit analysis. Compared with the original multiple-reflection method, the modified multiple-reflection method shows a dramatic increase in convergence speed. The validity of the nonlinear MESFET model is confirmed by comparing the simulation results with experimental data.**

I. INTRODUCTION

DUE TO THE excellent power performance of the GaAs MESFET, a wide range of power applications of GaAs MESFET's have been seen. The applications of the GaAs MESFET such as those in power amplifiers, oscillators, and mixers are growing rapidly.

Despite the demand for GaAs MESFET's as power devices, the large-signal design techniques for these circuits are in general still relatively primitive. A good large-signal model of the GaAs MESFET can aid the design of nonlinear MESFET circuits tremendously. Several research efforts have tried to develop numerical models of the GaAs MESFET [1]–[3]. These models use numerical techniques such as a finite-element method to solve the nonlinear differential equations that govern the physical properties of the device. These numerical models are valuable in understanding the device operation and can be used to aid the design of the MESFET itself. However, they are impractical for circuit-level design purposes due to the intensive computations required. Madjar and Rosenbaum [4], Shur [5], and Chua and Sing [6] developed approximate analytical models for the GaAs MESFET. With the exception of Madjar and Rosenbaum's model, none of these analytical models have shown validity in large-signal circuit design. Tajima *et al.* [7], [8] and Materka and Kacprzak [9] used a quasi-static approach to develop their circuit models. In this approach, the voltage dependencies of the nonlinear circuit elements at RF frequency are assumed to be the same as in the dc condition. They used the dc current–voltage characteristics and S-parameters versus bias voltage characteristics of the MESFET to establish the voltage dependencies of the nonlinear elements. Their results showed that this approach is accurate at least up to 18 GHz. In the present work, the circuit model employed in [9] is modified somewhat to better represent the device's behavior. A systematic, yet simple, technique of identifying the circuit elements and circuit parameter values is adopted.

The circuit model thus developed needs to be analyzed by a nonlinear circuit analysis routine. Frequently used nonlinear circuit analysis methods can be divided into two classes: time-domain analysis and hybrid analysis that iterates between the frequency and time domains. The time-domain approach includes the direct integration method and the shooting method. The direct integration method, such as the one used in SPICE, is a brute-force method and often requires excessive computation time when the transient time of the circuit under analysis is long. To avoid transient analysis, Colon and Trick [10] and Skelboe [11] proposed the shooting method, which yields the steady-state solution of the nonlinear circuit in the time domain. In the shooting method, the periodic solution $X(t)$ is sought to meet the two-point boundary condition $X(0) = X(T)$, where T is the period of the signal. The long transient response is avoided by updating $X(0)$ at the beginning of each iteration with an algorithm such as [10].

$$X^{k+1}(0) = X^k(0) - \left[X^k(0) - X^k(t)\right] / \left[1 - \partial X^k(T)/\partial X^k(0)\right] \quad (1)$$

where k indicates the iteration number. However, even with the shooting method, the computation time for the time-domain approach is long in general.

In the hybrid analysis approach, the circuit under analysis is decomposed into a nonlinear subcircuit and a linear subcircuit. The linear subcircuit is described by the linear equations in the frequency domain, and the nonlinear network is described by the nonlinear differential equations in the time domain. The goal is to find the steady-state solution of the voltages and/or currents at the nonlinear subcircuit/linear subcircuit interconnections, so that both sets of equations are satisfied simultaneously. The most

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often used hybrid analysis method is the harmonic balance method [12], [13]. In this algorithm, the voltages and/or currents at interconnections are optimized using numerical techniques such as the Newton-Raphson algorithm. The harmonic balance method can be quite efficient. However, the success of this approach often depends on good initial guess values. If the initial guess is poor, the solution might converge to local minimums or not converge at all.

Kerr [14] proposed a different kind of hybrid technique, which is called the multiple-reflection method. This method requires no initial guess. However, convergence is relatively slow. In the present work, the multiple-reflection technique is improved by incorporating a voltage update scheme [15] to accelerate the convergence. This modified multiple-reflection method is found to be more efficient than the original.

II. GaAs MESFET Modeling

The large-signal equivalent circuit shown in Fig. 1 is evolved from the conventional small-signal equivalent circuit. The parasitic inductances L_g, L_s, and L_d and the parasitic resistances R_s, R_g, and R_d do not exhibit strong bias dependency. These circuit elements are considered as linear elements. R_i is the charging resistance of the gate-to-source capacitance C_{gs}. Even though it has been reported that R_i exhibits a bias-dependent value [16], it is assumed to be a linear element in this work since its value is usually small. In our circuit model, C_{ds} consists of the drain and source electrodes' capacitance and the Gunn domain capacitance. For small V_{ds}, its value is expected to be small and is due only to the drain and source electrodes' capacitance. After saturation, its value increases due to the formation of the Gunn domain dipole layer. For simplicity, a constant value of C_{ds} is assumed in the saturation region in the present model.

The values of the parasitic resistances and inductances are determined by the self-consistent characterization technique [17]. The values of R_i and C_{ds} are optimized by the S-parameters at an arbitrarily chosen bias point in the saturation region.

The nonlinear circuit elements comprise I_{ch} (channel current), I_{br} (drain-to-gate breakdown current), I_f (forward-gate-bias current), C_{gs} (gate-to-source capacitance), and C_{gd} (gate-to-drain capacitance). The values of these nonlinear elements are determined by the quasi-static approach.

The nonlinear expressions for I_{ch} and I_{br} are determined by the dc drain current versus the drain and gate voltage dc curves. Fig. 2 shows the measured I–V curves of a Hughes MESFET which has 0.6-μm gate length and a 1-mm gate width. The total drain current is equal to the sum of the channel current and the breakdown current. The negative differential resistance observed at high gate voltage after saturation is often observed for short-gate GaAs MESFET's. The empirical expression for I_{ch} proposed by Materka and Kacprzak [9] is modified in incorporate this negative resistance phenomenon

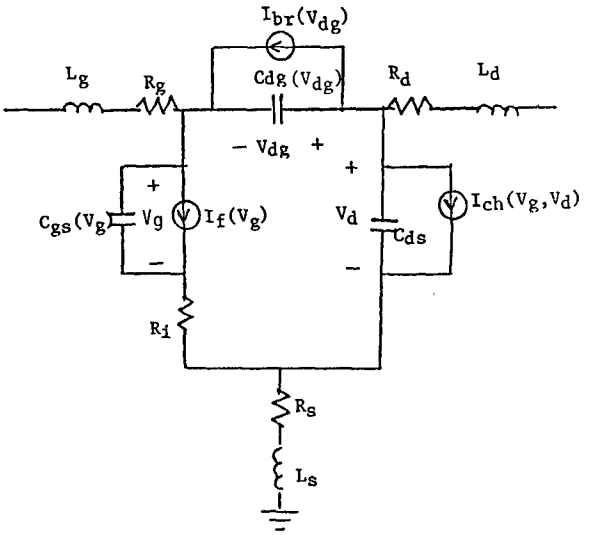

Fig. 1. Large-signal equivalent circuit of MESFET.

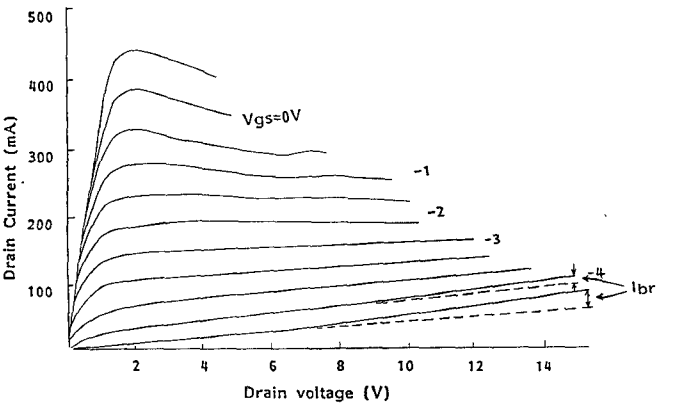

Fig. 2. Measured I–V curves of Hughes MESFET.

$$
\begin{aligned}
I_{ch}(t) &= I_{dss}\left[1 - V_g(t-\tau)/V_p\right]^2 \\
&\quad \cdot \tanh\left[c \cdot V_d / \left(V_g(t-\tau) - V_p\right)\right] \quad \text{for} \quad V_d < V_{\text{sat}} \\
&= I_{dss}\left[1 - V_g(t-\tau)/V_p\right]^2 \\
&\quad \cdot \tanh\left[c \cdot V_d / \left(V_g(t-\tau) - V_p\right)\right] \\
&\quad - V_d \cdot g_o / \left[V_s - V_g(t-\tau)\right]^q \quad \text{for} \quad V_d \geq V_{\text{sat}} \qquad (2)
\end{aligned}
$$

where $V_p = V_{po} + r \cdot V_d$. The fitting parameters I_{dss}, c, g_o, V_{po}, r, V_s, and V_{sat} are optimized to fit the measured I–V curves. V_g and V_d are as defined in Fig. 1. The parameter τ in (2) is the propagation delay time. The value of τ is assumed constant. This constant value of τ can be conveniently obtained by means of the small-signal equivalent circuit of the MESFET in Super-Compact [18], which has a time delay option. In this equivalent circuit, τ is optimized to fit measured S_{21} values at a normally biased condition (e.g., $V_{GS} = -2$ V, $V_{DS} = 7$ V for the Hughes MESFET). Greater accuracy is achieved by fitting S_{21} instead of all the S-parameters, since τ mainly affects the phase of S_{21}.

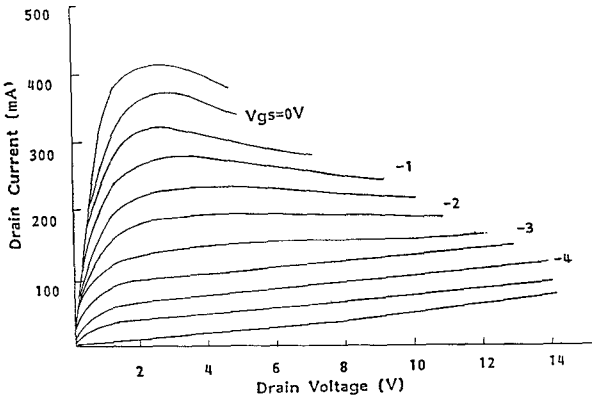

Fig. 3. Simulated $I-V$ curves of Hughes MESFET.

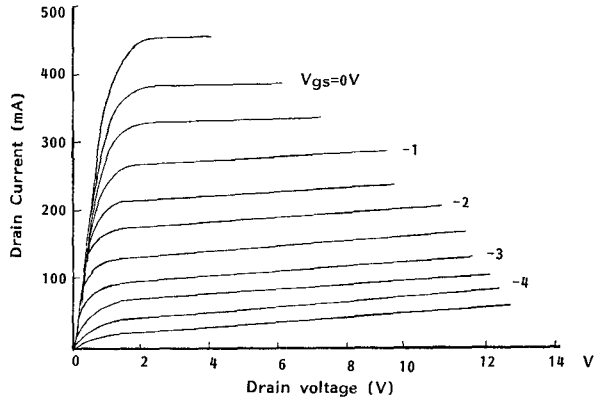

Fig. 4. $I-V$ curve of Hughes MESFET modeled by the expression of [9].

Tajima and Miller [8] reported an empirical model for I_{br}. Curtice and Ettenberg [13] used pulsed measurement of drain–gate avalanche current to find the parameters of Tajima and Miller's breakdown current model. For simplicity, the breakdown current is modeled as

$$I_{br} = I_{sr} \cdot \exp(\beta \cdot V_{dg}) \tag{3}$$

where V_{dg} is defined in Fig. 1. I_{sr} and β can be roughly estimated from the device's $I-V$ curves at the high drain voltage and low gate voltage region as shown in Fig. 2. Using these two empirical expressions, the simulated $I-V$ curves for the Hughes MESFET are shown in Fig. 3. For comparison, the original expression of [9] is also used to model the $I-V$ characteristics with the result shown in Fig. 4. In Section IV, it will be shown that neglecting the negative resistance phenomenon in RF large-signal simulation will tend to overestimate the output power in the saturation region of the device's power saturation curve.

The forward-gate-bias current is represented by

$$I_f = I_{so} \cdot \exp(\alpha \cdot V_g). \tag{4}$$

The values of I_{so} and α can be extracted by plotting gate current versus gate voltage with drain open.

The gate-to-source capacitance C_{gs} consists of two components:

$$C_{gs} = C_{sp} + C_{ss} \tag{5}$$

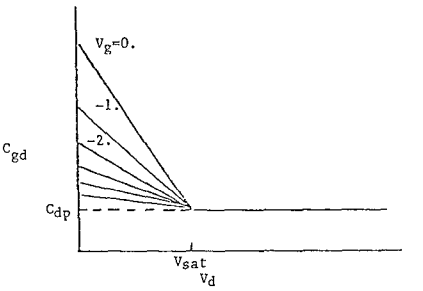

Fig. 5. Voltage dependency of C_{gd6}.

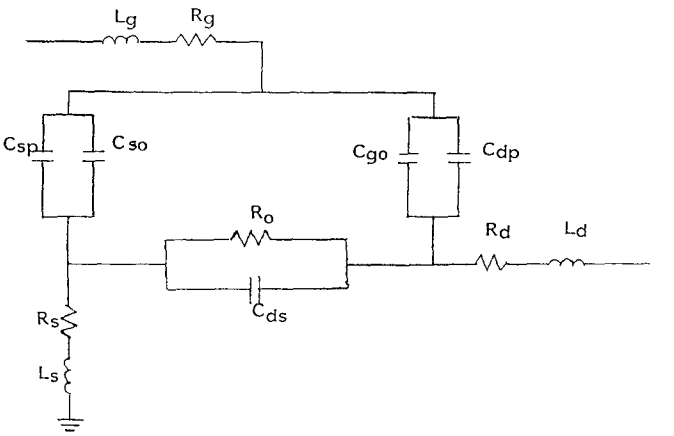

Fig. 6. Zero-biased equivalent circuit of MESFET.

where C_{sp} is the capacitance due to the gate and source contact metallization and C_{ss} is the gate-to-source depletion capacitance. Similarly, C_{gd}, the gate-to-drain capacitance, is expressed as

$$C_{gd} = C_{dp} + C_{dd} \tag{6}$$

where C_{dp} is the capacitance due to gate and drain contact metallization and C_{dd} is the gate-to-drain depletion capacitance. C_{ss} and C_{dd} together contribute to the total gate depletion capacitance. C_{dp} and C_{sp} can be conveniently calculated from the closed-form formula for coupled microstrip lines [19]. C_{ss} has been observed to be both gate voltage and drain voltage dependent [13] [16]. Since the drain-voltage dependency is relatively small, C_{ss} is assumed to be gate voltage dependent only, and is represented by the Schottky diode depletion capacitance expression. The total gate-to-source capacitance C_{gs} is

$$C_{gs} = C_{so}/(1 - V_g/V_b)^{1/2} + C_{sp}. \tag{7}$$

The gate-to-drain capacitance C_{gd} decreases rapidly as V_d increases in the linear region of $I-V$ curves. After saturation, the shape of the depletion region at the drain side does not change much as the drain voltage increases, and the C_{dd} becomes small. In this model, C_{dd} is assumed to decrease linearly to zero at the saturation voltage V_{sat}. The total gate-to-drain capacitance C_{gd} is modeled as

$$C_{gd} = C_{go}/(1 - V_g/V_b)^{1/2} \cdot (1 - V_d/V_{\text{sat}}) + C_{dp} \quad \text{for } V_d < V_{\text{sat}}$$
$$= C_{dp} \quad \text{for } V_d \geq V_{\text{sat}}. \tag{8}$$

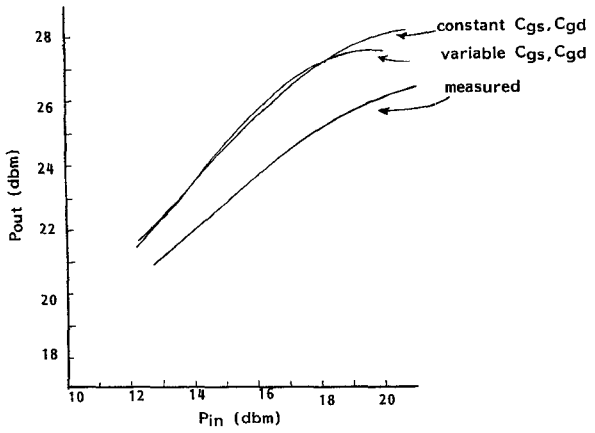

Fig. 7. RF output power versus input power calculated with variable C_{gs}, C_{gd} and with constant C_{gs}, C_{gd}.

The voltage dependency of C_{gd} is shown in Fig. 5. C_{so} of (7) and C_{go} of (8) can be optimized by means of the device's equivalent circuit (Fig. 6) and measured S-parameters at the zero-biased condition ($V_{GS} = 0$, $V_{DS} = 0$).

It has been reported [13] that C_{gs} and C_{gd} can be assumed to have constant values in calculating the RF power saturation characteristic. Our simulation of a device's RF saturation curve (Fig. 7) shows that this is true in general. However, in the saturation region, the deviation becomes larger, and it is more appropriate to use variable C_{gs} and C_{gd}.

III. Large-Signal Analysis

When the multiple-reflection method is used for MESFET analysis [20], [21], two ideal transmission lines are assumed to exist between the intrinsic MESFET circuit and the input–output embedding networks, as shown in Fig. 8. The parasitic resistances and inductances at the drain and gate sides are absorbed into the embedding circuit. The transmission lines have lengths equal to large integer multiples of the fundamental wavelength. Because of the above assumptions, the intrinsic MESFET circuit and the matching circuit can be analyzed iteratively and the insertion of these two transmission lines does not affect the steady-state solution. The choices of the characteristic impedances of the transmission lines affect the convergence speed. Mass discussed the criteria of chosing these characteristic impedances [21]. In general, the characteristic impedances should be chosen to match the input and output termination impedances, so that minimum reflection occurs. The multiple-reflection algorithm is illustrated in Fig. 9. At the first iteration, the initial incident wave $V_{ii}^1(t)$ due to the input RF voltage source and gate bias voltage and the $V_{Li}^1(t)$ due to the drain bias voltage are calculated. The superscript indicates iteration number. These voltage waves travel the length of the transmission lines and are applied to the intrinsic MESFET circuit. Then, the intrinsic MESFET circuit is analyzed in the time domain. After the MESFET circuit reaches steady state, the voltage waves reflected from the MESFET circuit are calculated. The reflected waves at input and output can be represented by Fourier series summation:

$$Vir^1(t) = \sum_{n=0}^{\infty} V_{ir}^1(n\omega)e^{jn\omega t}$$

$$V_{Lr}^1(t) = \sum_{n=0}^{\infty} V_{Lr}^1(n\omega)e^{jn\omega t}, \qquad n = 0,1,2,\cdots. \quad (9)$$

Let the operators of calculation $V_{ir}^k(n\omega)$ and $V_{Lr}^k(n\omega)$ be $F_i\{\}$ and $F_L\{\}$, respectively; then

$$V_{ir}^k(n\omega) = F_i\{V_{ii}^k(t), V_{Li}^k(t)\}$$

$$V_{Lr}^k(n\omega) = F_L\{V_{ii}^k(t), V_{Li}^k(t)\} \quad (10)$$

where k indicates the iteration number. These reflected waves travel back to the input/output matching circuits and are reflected again. The new incident waves are now equal to these reflected waves plus the initial incident waves

$$V_{ii}^2(t) = V_{ii}^1(t) + \sum_{n=1}^{\infty} V_{ir}^1(n\omega)\Gamma_i(n\omega)e^{jn\omega t}$$

$$V_{Li}^2(t) = V_{Li}^1(t) + \sum_{n=1}^{\infty} V_{Lr}^1(n\omega)\Gamma_L(n\omega)e^{jn\omega t} \quad (11)$$

where $\Gamma_i(n\omega)$ and $\Gamma_L(n\omega)$ are the reflection coefficients at the interfaces of the transmission lines and the input/output matching networks, respectively. The iteration continues until the solution converges to a steady-state value. Unlike the harmonic balance method, the multiple-reflection method does not need an initial guess. Also, it does not use a numerical optimization scheme. The starting values of iteration are just the first incident waves calculated. The iteration scheme preserved the physical nature of wave traveling and reflection.

Hicks and Khan [15] proposed a voltage-update algorithm to analyze a Schottky-diode circuit. This voltage-update scheme can be incorporated into the multiple-reflection method to accelerate the convergence. In this modified multiple-reflection method, the reflected voltage waves are calculated as

$$V_{ir}^k(m\omega) = V_{ir}^{k-1}(m\omega) + P_m\left(F_i\{V_{ii}^k(t), V_{Li}^k(t)\} - V_{ir}^{k-1}(m\omega)\right)$$

$$V_{Lr}^k(m\omega) = V_{Lr}^{k-1}(m\omega) + P_m\left(F_L\{V_{ii}^k(t), V_{Li}^k(t)\} - V_{Lr}^{k-1}(m\omega)\right),$$

$$0 < P_m \le 1, \; m = 0,1,2,\cdots \quad (12)$$

where $F_i\{\}$ and $F_L\{\}$ are the same operations as defined in (11).

The values of P_m affect the speed of convergence. The optimum values of P_m depend upon the FET's nonlinearity. Typically, the optimum P_m values are found to be 0.5. The standard multiple-reflection method results with $P_m = 1$. Convergence is checked by comparing the rms difference of the reflected waves in the time domain of two consecutive iterations. The steady-state solution is considered to be reached when the rms differences at both input and output are less than some specified tolerance values.

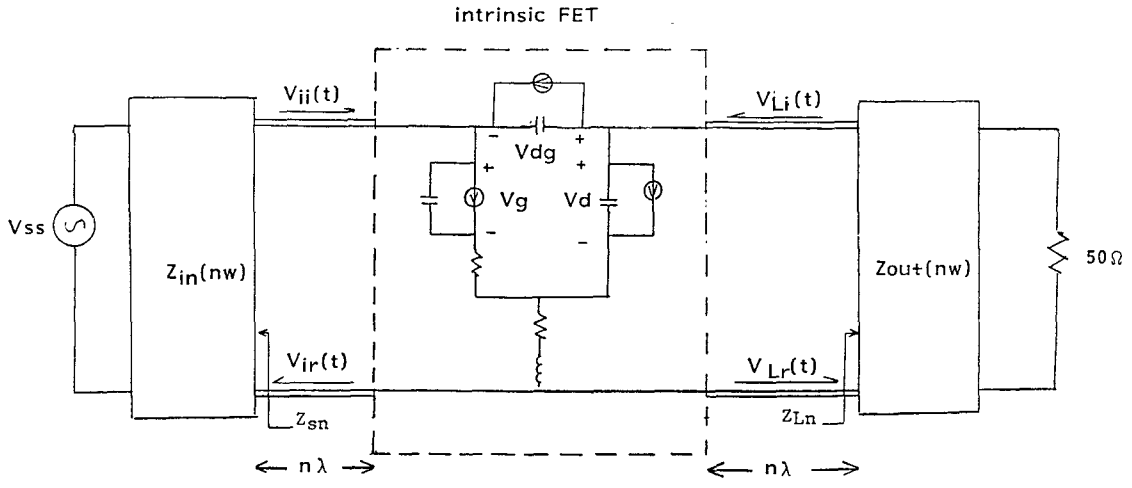

Fig. 8. Schematic diagram of large-signal analysis.

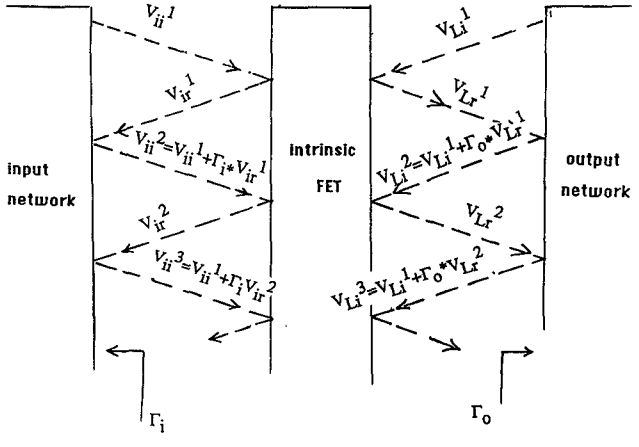

Fig. 9. Multiple-reflection scheme.

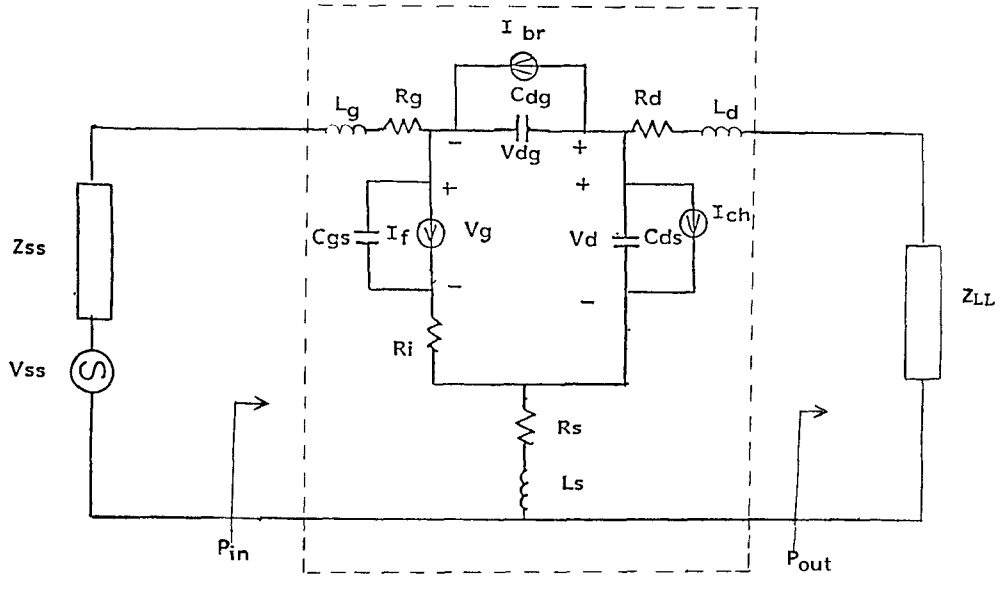

Fig. 10. Simplified amplifier configuration.

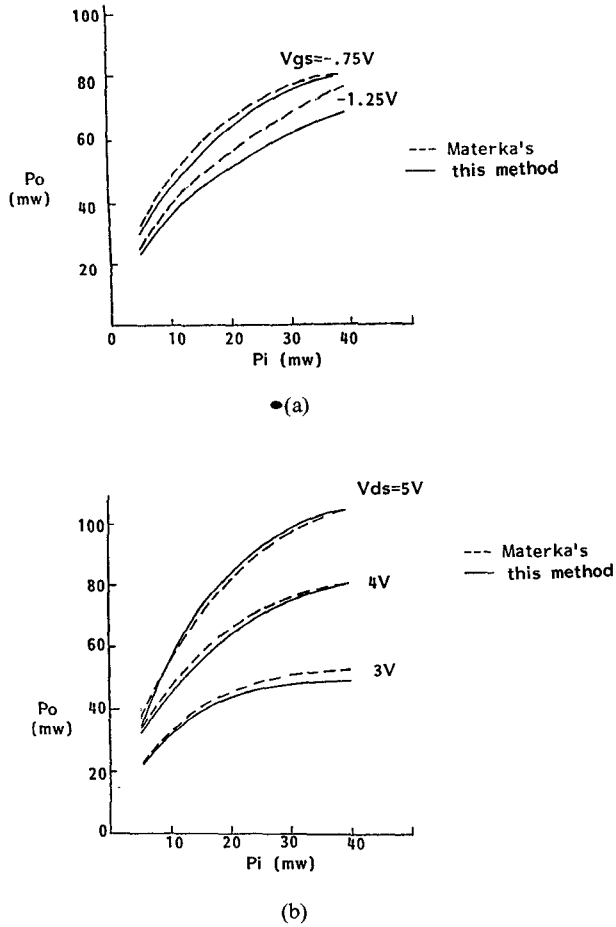

Fig. 11. (a) Output power versus input power of Materka's amplifier, $V_{DS} = 4$ V. (b) Output power versus input power of Materka's amplifier, $V_{GS} = -0.75$ V.

TABLE I
MODEL PARAMETERS FOR HUGHES MESFET

R_S	.75 Ω	C_{ds}	.4pf	g_0	.279	I_{sr}	.13mA
R_d	.80Ω	C_{sp}	.079pf	q	2.56	β	.231
R_g	1.14Ω	C_{so}	.48pf	V_{po}	-5.28v	I_{so}	1.05 pA
R_i	.65 Ω	C_{go}	.48pf	γ	-.227	α	34
L_s	.012nH	C_{dp}	.079pf	V_s	2.23		
L_d	.092nH	I_{dss}	496mA	V_{sat}	1.85		
L_g	.127nH	c	4.52	τ	4.7ps		

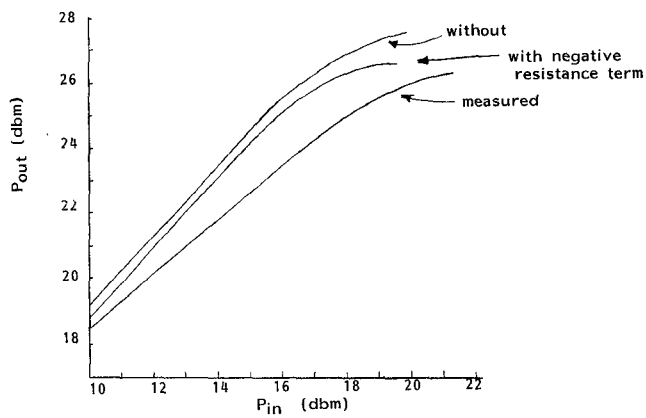

Fig. 12. Output power versus input power curve of Hughes MESFET amplifier $V_{DS} = 7$ V, $V_{GS} = -2.03$ V, $f = 15$ GHz, $Z_{SS} = 50$ Ω, $Z_{LL} = 11 + 8.5j$.

In the simulations of Section IV, a relative tolerance of 0.5 percent is used. To save computation time, when using the modified multiple-reflection method, the previous solution can be used as the initial guess if the operating condition is changed by a small amount. However, it is not necessary to do so to ensure convergence in this method.

IV. Large-Signal Simulations

To check the validity of the modified multiple-reflection method, the MESFET amplifier simulation in [9] is repeated using the modified multiple-reflection method. The device is simulated in the amplifier configuration shown in Fig. 10. The results of [9], which are obtained by the harmonic balance method, are compared to the results obtained by the present method in Fig. 11. By means of the modified multiple-reflection method, the solution to this particular simulation usually converges within five iterations. When the original multiple-reflection method is used, the solutions converge only after 18 iterations.

A Hughes MESFET with 0.6-μm gate length and a 1-mm gate width is modeled in this work. With the techniques stated earlier, the circuit parameters are obtained and are listed in Table I. This MESFET is also simulated in an amplifier configuration. Curtice and Ettenberg [13] have stressed the importance of including the harmonic termination impedances in large-signal simulation. In this calculation, the fundamental and second harmonic are taken into account. The input is simulated with a 50-Ω termination and the output has an $11 + 8.5j$ termination impedance at the 15-GHz fundamental frequency. The second harmonic termination impedances for this calculation assume lumped-element matching. Both the expression of [9] and our expression, which includes a negative resistance term for channel current, $-I_{ch}$, are used for calculating the amplifier power saturation curve. The input power P_{in} and the output power P_{out} are defined in Fig. 10. The results are compared with the measured data in Fig. 12. Even though both curves predict higher power output than the measured curve, the discrepancy becomes smaller in the saturation region for our representation, which includes the negative resistance term. The lower measured power can partially contribute to the power loss in the input tuner used in the power measurement. The method here takes an average of seven iterations to converge, whereas the original multiple-reflection method does not converge even after 50 iterations.

The multiple-reflection method works well when the termination impedances are matched, as in the first simulation. When the termination impedances are not matched to the MESFET, as in the second case, where the input has a 50-Ω termination, the multiple-reflection method runs

into a convergence problem. The modified multiple-reflection method shows good convergence speed in both cases.

V. Conclusions

The modified multiple-reflection method is shown to be an efficient nonlinear circuit simulation algorithm. It is applied successfully to the large-signal MESFET circuit analysis. A useful computer-aided design tool can be developed by automating the procedures of extracting MESFET circuit model elements, and linking the result with the present nonlinear circuit analysis algorithm and a linear circuit simulation program such as Super-Compact.

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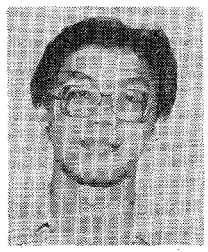

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